REMARKS

Claims 29-54 are pending in this application. Claim 36 has been amended.

Claims 36-46 stand rejected under 35 U.S.C. §112, second paragraph, as being "indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." (Office Action at 2). Independent claim 36 has been amended to correct any perceived indefiniteness. Applicant notes that all pending claims are now in full compliance with 35 U.S.C. §112.

The drawings stand objected to under 37 CFR 1.83(a) "because they fail to show the limitation of 'said electrode having a surface aligned over said source/drain region,' as described in claim 36." (Office Action at 2). As noted above, independent claim 36 has been amended to recite that the electrode is "being in electrical contact with said source/drain region." Accordingly, the drawings are now in full compliance with 37 CFR 1.83(a).

Claims 29, 35-36 and 42-43 stand rejected under 35 U.S.C. §102 as being anticipated by Jeng et al. (U.S. Patent No. 6,184,081) ("Jeng"). This rejection is respectfully traversed.

The claimed invention relates to an electropolished patterned metal layer formed as part of a semiconductor device. As such, independent claim 29 recites a "semiconductor device" comprising a substrate and "an electropolished patterned metal layer provided over said substrate." Amended independent claim 36 recites a "memory cell" comprising "an electropolished patterned metal layer provided over a semiconductor substrate," "a transistor in electrical communication with said electropolished patterned metal layer" including a gate and a source/drain region, and "a capacitor including an electrode, said electrode being in electrical contact with said source/drain region."

Jeng relates to a method of forming an upper plate of a capacitor "simultaneously with the opening of bit line, and substrate, contact hole openings, using

the same photolithographic mask and dry etching procedures." (Col. 1, lines 62-65). For this, Jeng teaches "isolating a polysilicon upper plate structure (23a), during an isotropic RIE cycle, also creating an undercut polysilicon region, in the contact holes (28a) (29a), which are opened simultaneously during the upper plate (23b) formation." (Abstract; Figures 6-8). Jeng teaches that the upper capacitor plate (23b) is formed of polysilicon and that the lower capacitor plate is formed of a polysilicon layer (19) and a conductive layer (20), which may be "an in situ doped polysilicon layer, a tungsten layer, or a titanium nitride layer." (Col. 4, lines 21-38; Figure 8).

Jeng does not teach or suggest the limitations of the claimed invention. Jeng does not disclose "an *electropolished patterned* metal layer" as part of a semiconductor device, as independent claim 29 and amended independent claim 36 recite. As noted above, Jeng teaches an isotropic RIE cycle for creating an undercut polysilicon region in the contact holes (28a) (29a) which are opened simultaneously during the upper plate (23b) formation" (Abstract; Figures 6-8), and not "an electropolished patterned metal layer," as in the claimed invention. For at least these reasons, Jeng fails to disclose all limitations of claims 29, 35-36 and 42-43 and withdrawal of the rejection of these claims is respectfully requested.

Claims 30-34, 37-41 and 44-54 stand rejected under 35 U.S.C. §103 as being unpatentable over Jeng et al. (U.S. Patent No. 6,184,081) ("Jeng") in view of McClure et al. (U.S. Patent No. 6,027,860) ("McClure"). This rejection is respectfully traversed.

McClure relates to a "method of forming a structure by redepositing a starting material on sidewalls of a foundation during an etch of the starting material." (Abstract). McClure teaches that the conductive layer to be etched may be formed of "platinum, conductive oxides, and polysilicon." (Col. 3, lines 33-35).

The subject matter of claims 30-34, 37-41 and 44-54 would not have been obvious over Jeng in view of McClure. Indeed, the Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie*

case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 U.S.P.Q.2d 1626, 1630 (Fed. Cir. 1996).

In the present case, neither Jeng nor McClure, whether considered alone or in combination, teach or suggest the limitations of claims 30-34, 37-41 and 44-54. Jeng is silent about "an *electropolished patterned* metal layer" as part of a semiconductor device, as amended independent claim 36 and independent claim 44 recite. As noted above, Jeng teaches "an undercut polysilicon region in the contact holes (28a) (29a) which are opened simultaneously during the upper plate (23b) formation" (Abstract; Figures 6-8), and not "an electropolished patterned metal layer," as in the claimed invention. Similarly, McClure is silent about a patterned metal layer, much less about "an electropolished patterned metal layer," as in the claimed invention. The crux of McClure is a "redeposited" starting conductive material, which may be part of a capacitor structure, and not "an electropolished patterned metal layer," as in the claimed invention.

In addition, a person of ordinary skill in the art would not have been motivated to combine the teachings of McClure with those of Jeng because no suggestion or motivation to combine the references exists. Courts have generally held that, to establish a *prima facie* case of obviousness, "[I]t is insufficient that the prior art disclosed the components of the patented device, either separately or used in other combinations; there must be some teaching, suggestion, or incentive to make the combination made by the inventor." Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934, 15 U.S.P.Q.2d 1321, 1323 (Fed. Cir. 1990). This way, "the inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a

whole for which patentability is claimed." Hartness Int'l, Inc. v. Simplimatic Engineering Co., 819 F.2d 1100, 1108, 2 U.S.P.Q.2d 1826, 1832 (Fed. Cir. 1987). Accordingly, a determination of obviousness "must involve more than indiscriminately combining prior art; a motivation or suggestion to combine must exist." Pro-Mold & Tool Co., 75 F.3d at 1573.

As noted above, the crux of Jeng is a method of forming a capacitor upper plate "simultaneously with the opening of bit line, and . . . contact hole openings." (Col. 1, lines 62-65). For this, Jeng teaches a sequence of processing steps for the formation of polysilicon upper plate (23b) and of the contact holes (28a), (29a). (Abstract; Figures 6-8). In contrast, the crux of McClure is a method of "redepositing a starting material on sidewalls of a foundation during an etch of the starting material" (abstract), with the etch creating "particles or portions of each layer which are then deposited on sidewalls of the foundation." (Col. 1, lines 44-46). Thus, it is clear that the only structure that Jeng and McClure have in common is the semiconductor wafer on which their respective methods take place. Accordingly, a person skilled in the art would not have been motivated to combination the two references, and withdrawal of the rejection of claims 30-34, 37-41 and 44-54 is respectfully requested.

A marked-up version of the changes made to the claims by the current amendment is attached. The attached page is captioned "**Version with markings to show changes made.**"

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: July 26, 2002

Respectfully submitted,

By_____

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Version With Markings to Show Changes Made

36. (Amended) A memory cell comprising:

an electropolished patterned metal layer provided over a semiconductor substrate;

a transistor in electrical communication with said electropolished patterned metal layer, said transistor including a gate fabricated on said semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate; and

a capacitor including an electrode, said electrode [having a surface aligned over] being in electrical contact with said source/drain region.